GRID ARRAY MICROELECTRONIC PACKAGES WITH INCREASED PERIPHERY

Abstract of the Disclosure

A grid array microelectronic package includes a substrate and an array of external connectors on the substrate that are arranged in rows and columns to define a periphery of the array and the interior of the array. A routing channel is provided in the array that increases the periphery of the array by at least four external connectors, compared to absence of the routing channel. The routing channel may be made of two missing external connectors, at least two strapped external connectors and/or at least two "no-connect" external connectors in the array that extend from the periphery of the array towards the interior of the array. Signal conductors may extend along the routing channel.